FIG.1
PRIOR ART

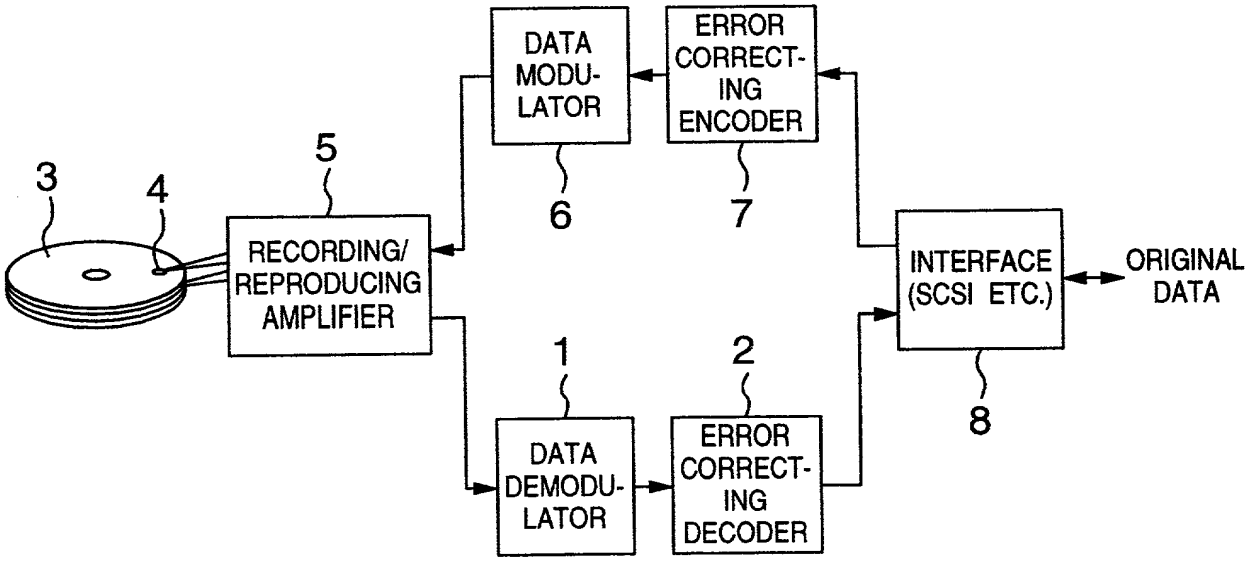


FIG.2

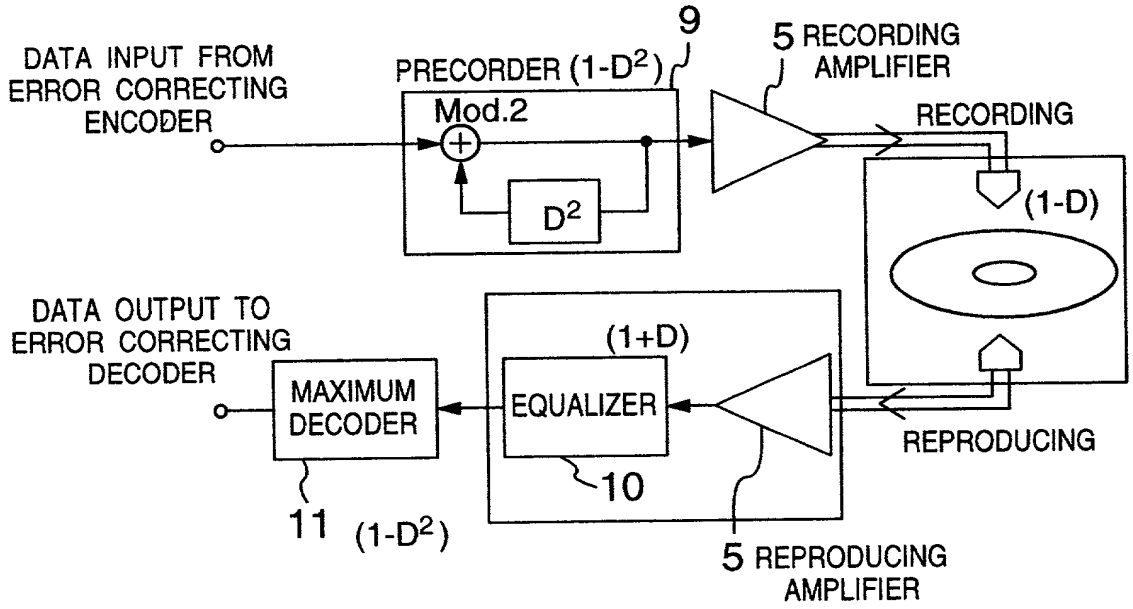


FIG.3A PRIOR ART

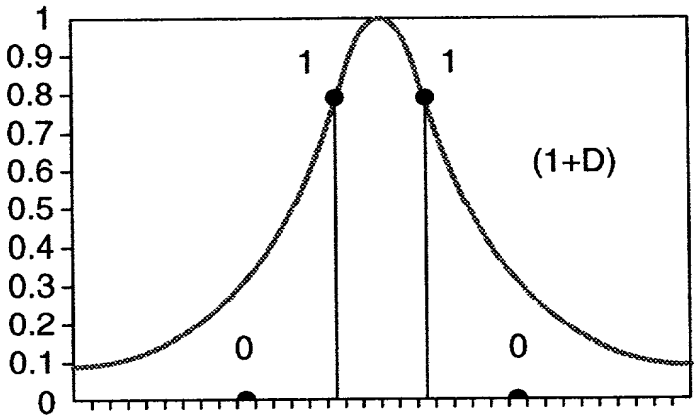


FIG.3B PRIOR ART

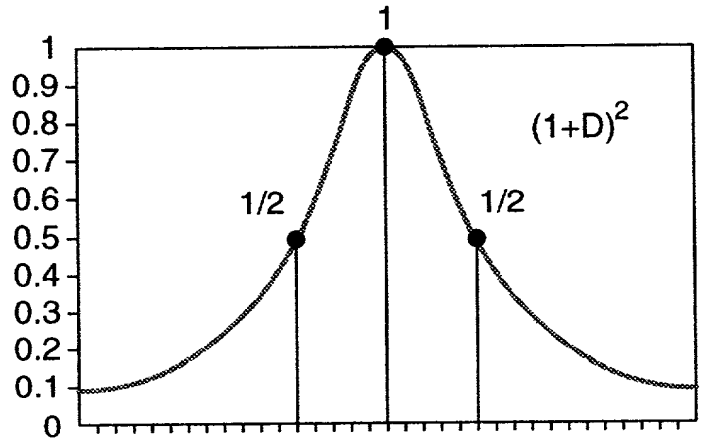


FIG.3C PRIOR ART

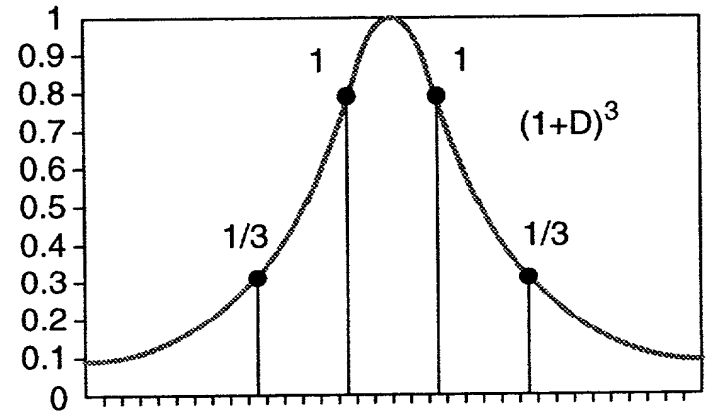


FIG.4
PRIOR ART

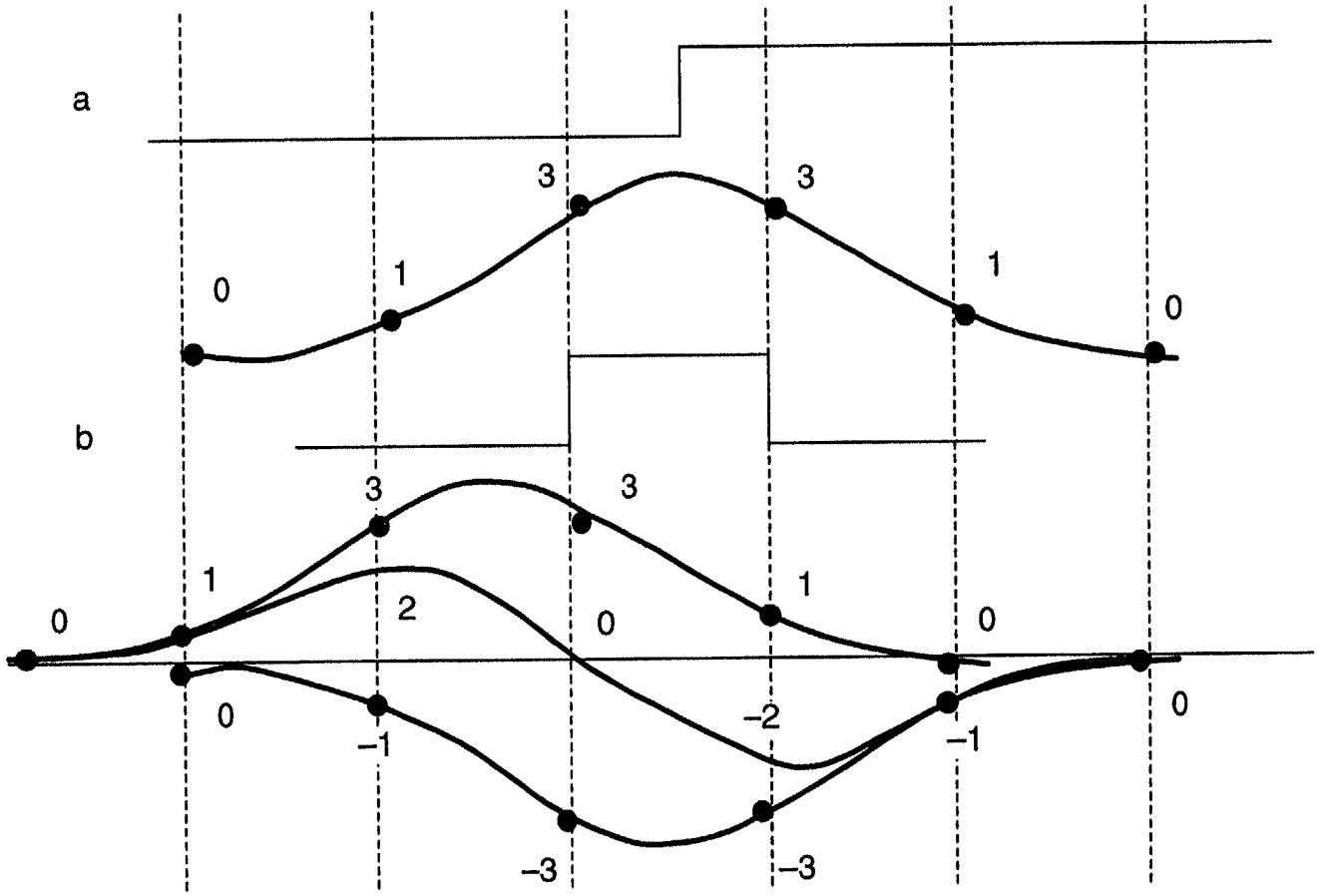
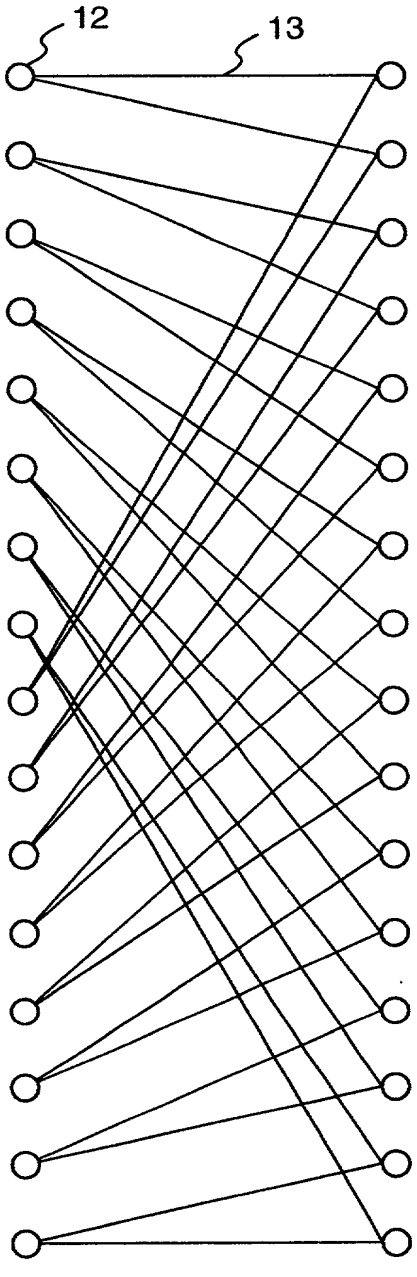


FIG.5
PRIOR ART

S_k	a_k / y_k
0000	0 / " 0 " 1 / " 1 "
0001	0 / " 2 " 1 / " 3 "
0010	0 / " 0 " 1 / " 1 "
0011	0 / " 2 " 1 / " 3 "
0100	0 / " −2 " 1 / " −1 "
0101	0 / " 0 " 1 / " 1 "
0110	0 / " −2 " 1 / " −1 "
0111	0 / " 0 " 1 / " 1 "
1000	0 / " −1 " 1 / " 0 "
1001	0 / " 1 " 1 / " 2 "
1010	0 / " −1 " 1 / " 0 "
1011	0 / " 1 " 1 / " 2 "
1100	0 / " −3 " 1 / " −2 "
1101	0 / " −1 " 1 / " 0 "
1110	0 / " −3 " 1 / " −2 "
1111	0 / " −1 " 1 / " 0 "

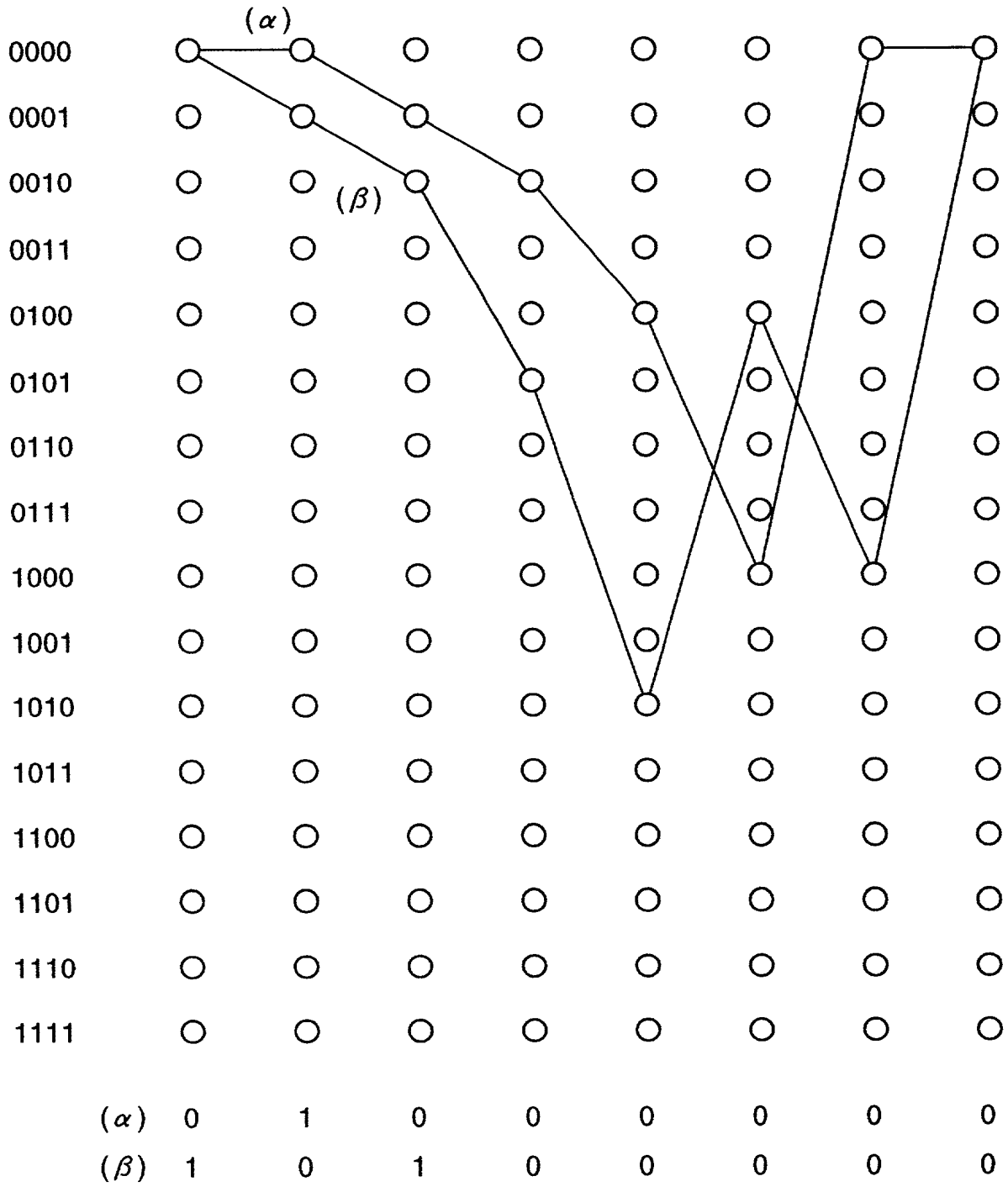


$$y_k = a_k + 2a_{k-1} - 2a_{k-3} - a_{k-4}$$

$$s_k = a_{k-4} a_{k-3} a_{k-2} a_{k-1}$$

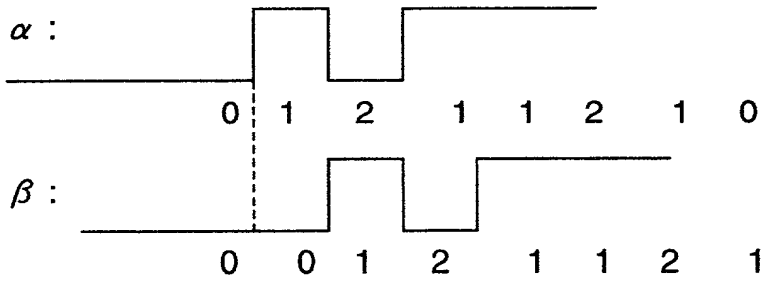
EP 0 696 125 A1

FIG.6
PRIOR ART



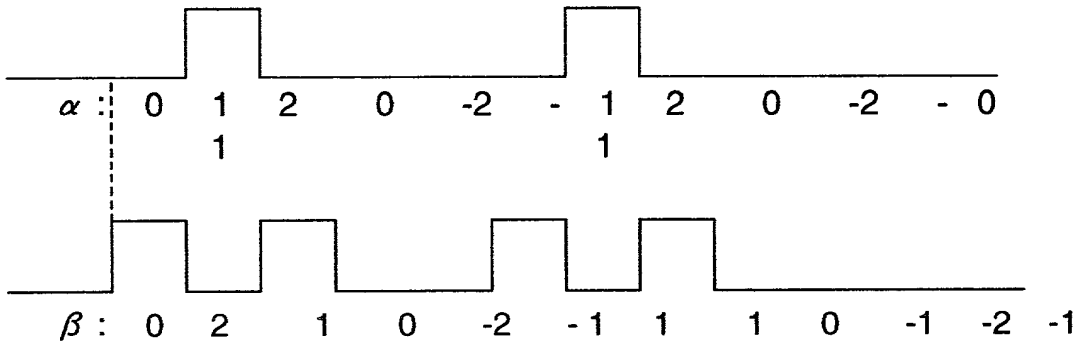
0000025.11.2001

FIG.7



$$(\alpha-\beta)^2 = (1-0)^2 + (2-1)^2 + (1-2)^2 + (1-1)^2 + (2-1)^2 + (1-2)^2 + (0-1)^2$$
$$= 6$$

FIG.8



$$(\alpha-\beta)^2 = 8$$

FIG.9A

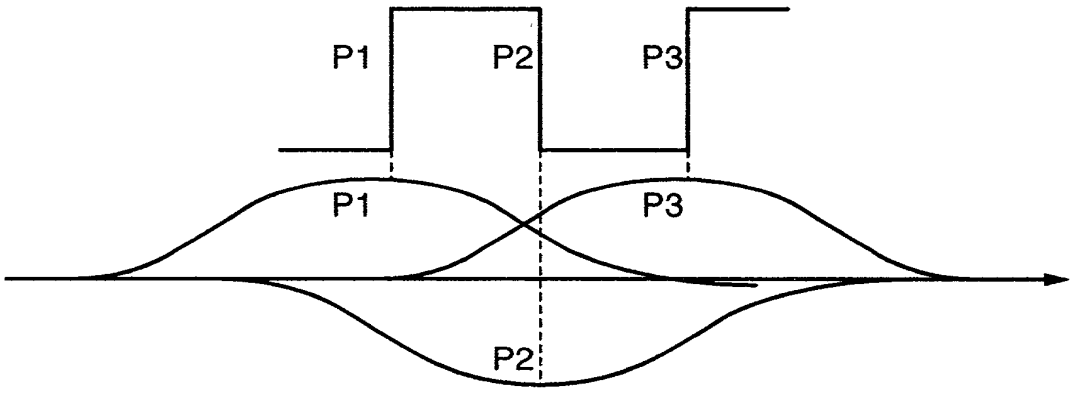


FIG.9B

(a)	1	3	3	1			
			1	3	3	1	
		−1	−3	−3	−1		
	1	2	1	1	2	1	

(b)	1	3	3	0			
			1	3	3	0	
		−1	−3	−3	0		
	1	2	1	0	3	0	

FIG.10

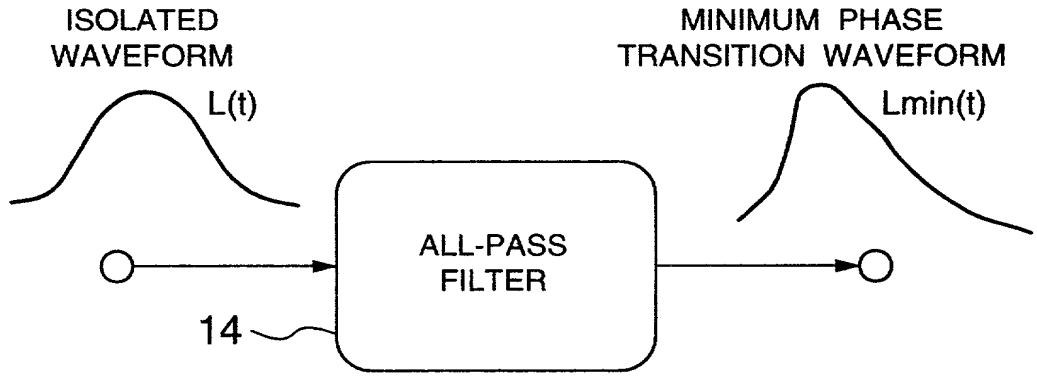


FIG.11

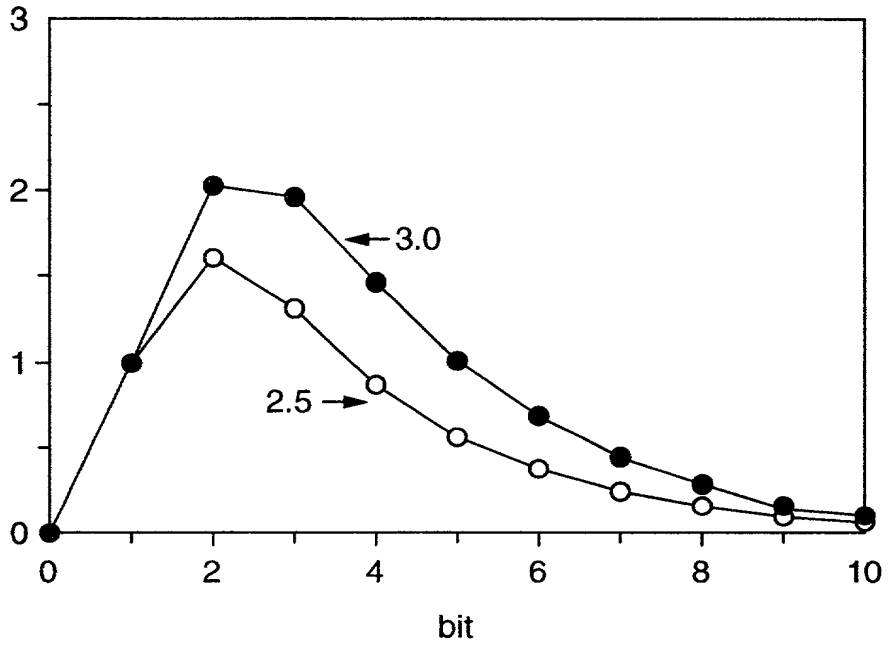

3
2
1
0
3.0
2.5
0
2
4
6
8
10
bit

FIG.12

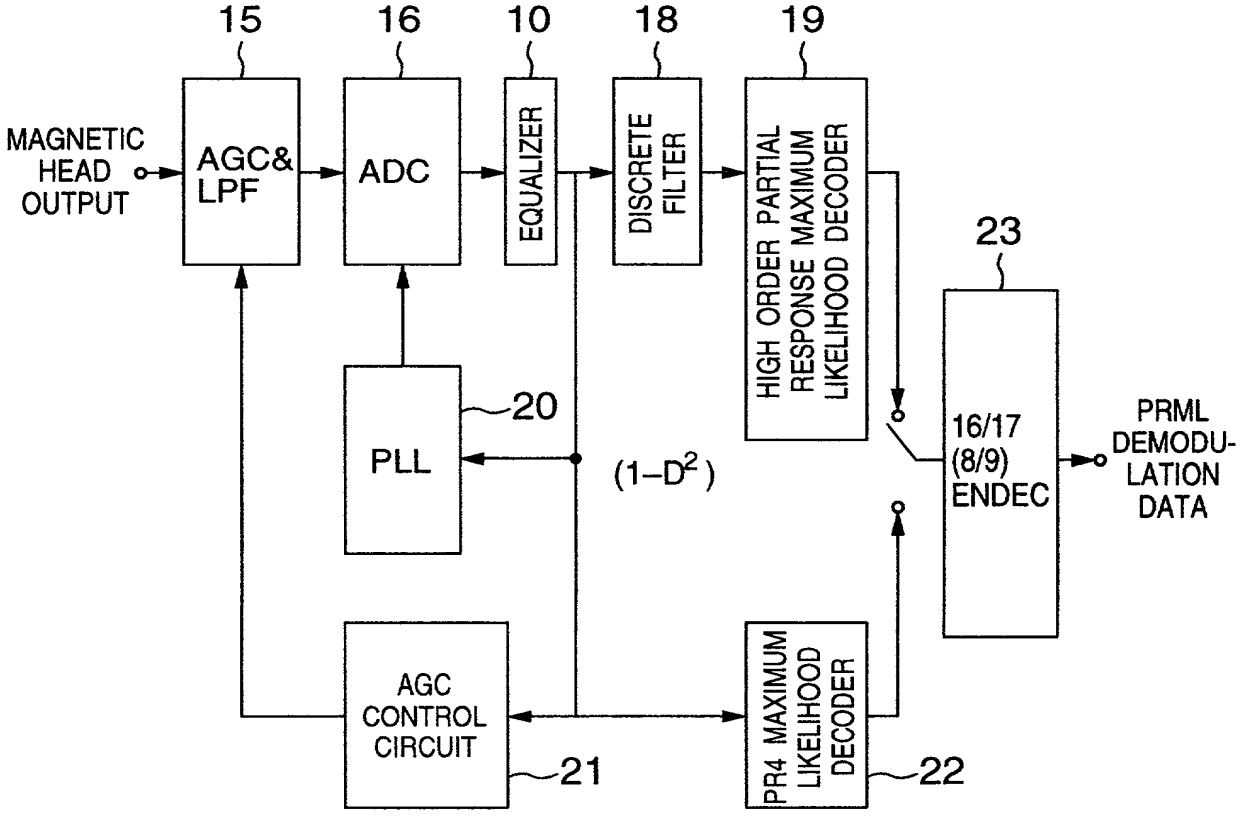
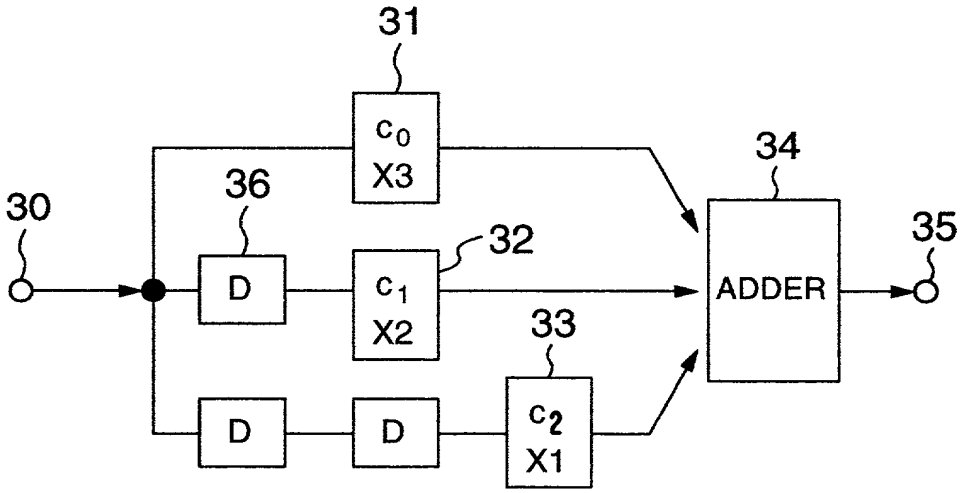

15
16
10
18
19
MAGNETIC HEAD OUTPUT
AGC& LPF
ADC
EQUALIZER
DISCRETE FILTER
HIGH ORDER PARTIAL RESPONSE MAXIMUM LIKELIHOOD DECODER
23
PLL
20
(1–D²)
16/17 (8/9) ENDEC
PRML DEMODU-LATION DATA
AGC CONTROL CIRCUIT
21
PR4 MAXIMUM LIKELIHOOD DECODER
22

FIG.13A



D : 1-BIT DELAY CIRCUIT

FIG.13B

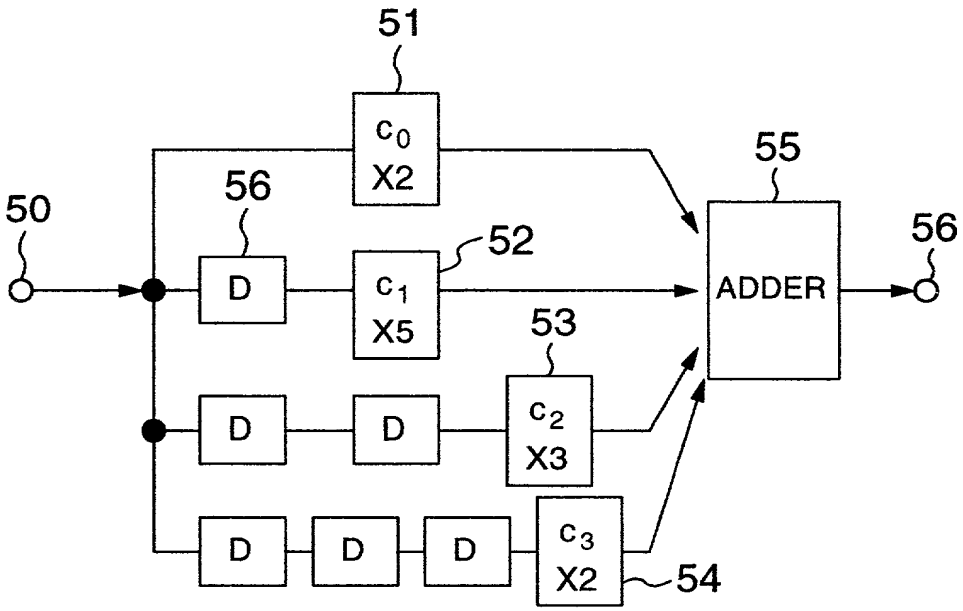
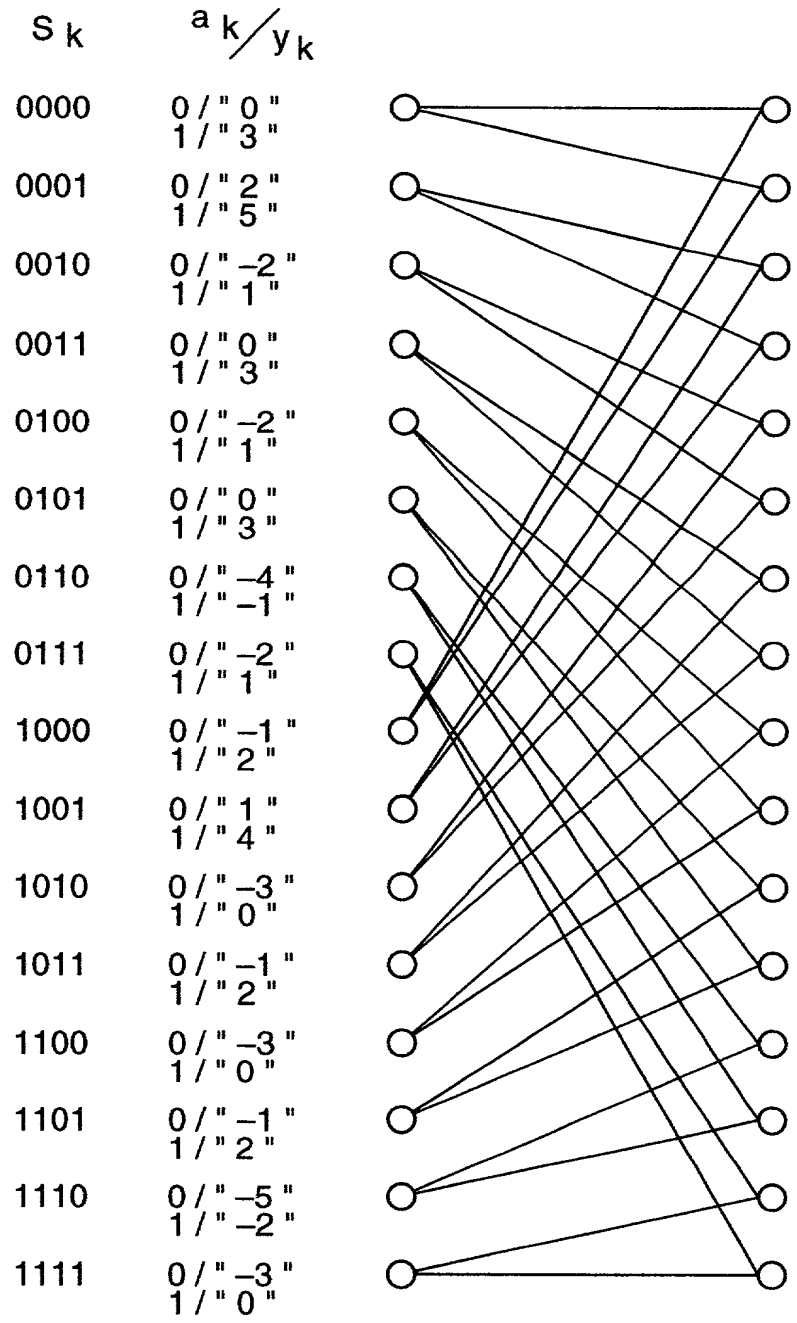


FIG.14



$y_k = 3a_k + 2a_{k-1} - 2a_{k-2} - 2a_{k-3} - a_{k-4}$

$s_k = a_{k-4} a_{k-3} a_{k-2} a_{k-1}$

EP 0 954 174 A1

FIG.15

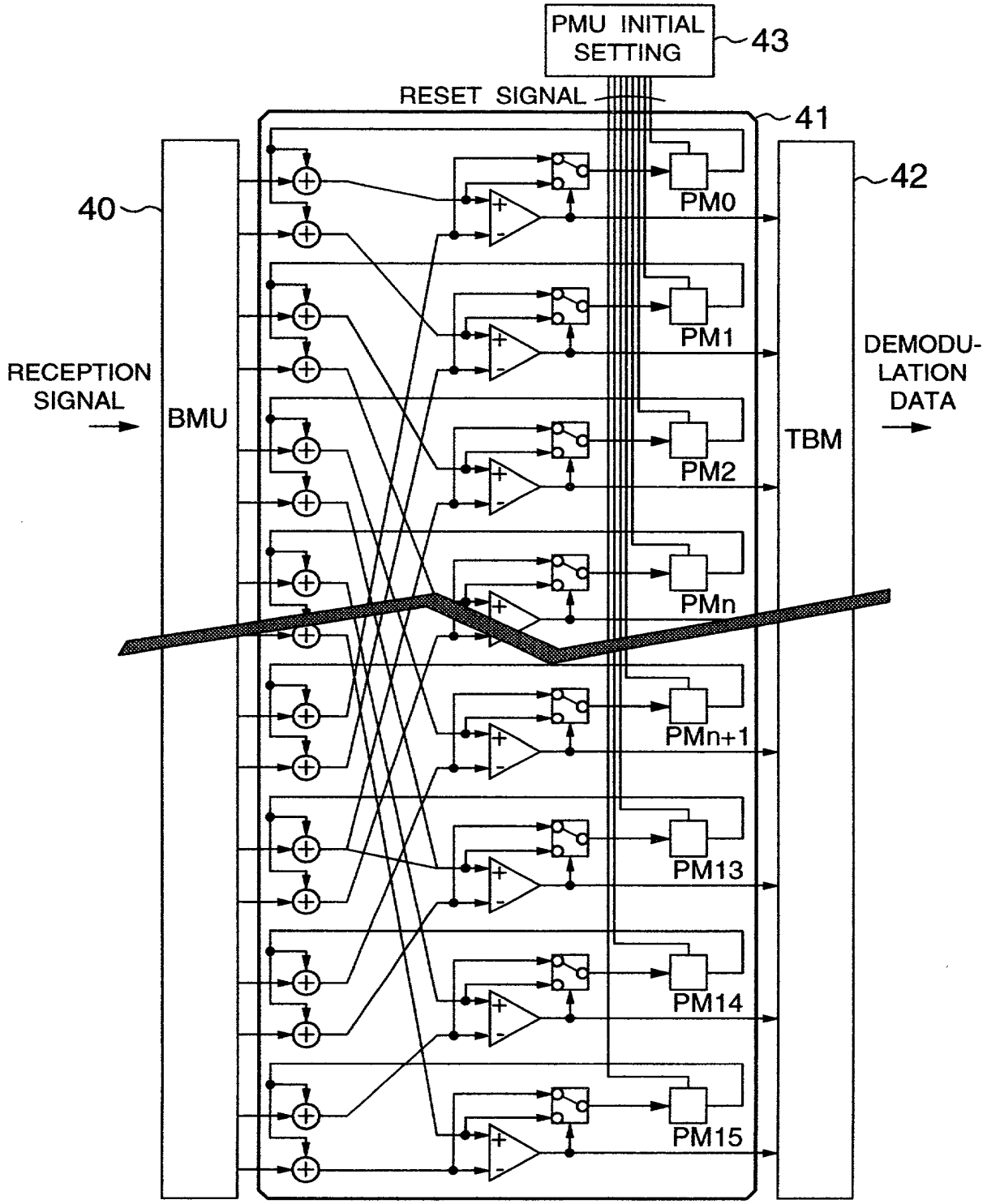
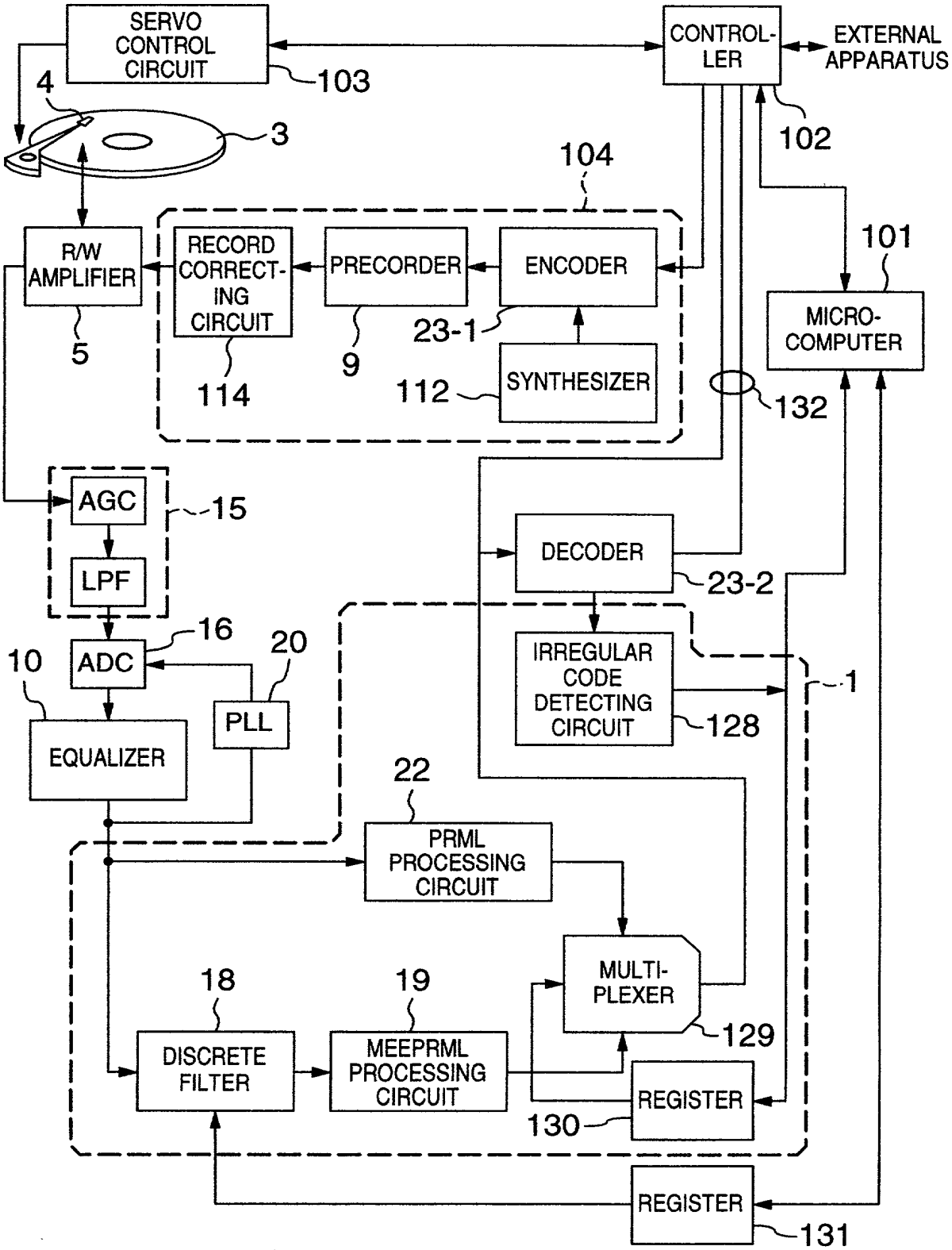

PMU INITIAL SETTING
43
RESET SIGNAL
41
40
42
RECEPTION SIGNAL
BMU
TBM
DEMODU-LATION DATA
PM0
PM1
PM2
PMn
PMn+1
PM13
PM14
PM15

FIG.16


SERVO CONTROL CIRCUIT
103
CONTROL-LER
EXTERNAL APPARATUS
102
4
3
104
101
R/W AMPLIFIER
5
RECORD CORRECT-ING CIRCUIT
114
PRECORDER
9
ENCODER
23-1
SYNTHESIZER
112
MICRO-COMPUTER
132
AGC
15
LPF
DECODER
23-2
16
20
10
ADC
PLL
EQUALIZER
IRREGULAR CODE DETECTING CIRCUIT
128
1
22
PRML PROCESSING CIRCUIT
MULTI-PLEXER
129
18
19
DISCRETE FILTER
MEEPRML PROCESSING CIRCUIT
REGISTER
130
REGISTER
131